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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
SONG, HOON K

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/001,438	Applicant(s) LYON ET AL.	
	Examiner Hoon K Song	Art Unit 2882	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Figure 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoneyama (US 6480227B1).

Regarding claims 1, 28, 29, Yoneyama teaches an image sensor (figure 2), comprising:

a plurality of active pixel sensors arranged in a plurality of rows and at least one column, each active pixel sensor including a photo-sensor configured to generate a sensor signal nominally indicative of an intensity of light incident on the photo-sensor (figure 2);

a follower-type amplifier (QAij) configured to provide a buffered sensor signal based on the sensor signal (column 8 line 47+); and

sensor output selection circuitry configured to selectively couple the buffered sensor signal to an output of the active pixel sensor when the row to which the active pixel sensor belongs is selected based on one of a set (composite signal, column 3 line 38+) of row select signals corresponding to that row;

for each column, a column line coupling together the outputs of the active pixel sensors that belong to that column (figure 2); and

row select signal generating circuitry configured to generate the set of row select signals to substantially simultaneously select a corresponding set of plural particular rows such that each of the active pixel sensors in the selected corresponding set of plural particular rows substantially simultaneously provides the buffered sensor signal for that active pixel sensor to the column line for the column to which that active pixel sensor belongs such that an output node of each column line indicates a collective output signal for the active pixel sensors in that selected corresponding set of plural particular rows, belonging to that column (column 3 line 60+).

Regarding claim 2, Yoneyama teaches that the follower-type amplifier includes a field-effect transistor configured as a source-follower amplifier (column 8 line 47+).

Regarding claim 3, Yoneyama teaches that: the sensor output selection circuitry includes a field-effect transistor, wherein the gate of the sensor output selection circuitry field-effect transistor is coupled to the one of the set of row select signals; and the

source-follower amplifier field-effect transistor and the sensor output selection circuitry field-effect transistor each have the same conductivity type (column 8 line 47+).

Regarding claim 4, Yoneyama teaches that: the follower-type amplifier includes a bipolar transistor configured as an emitter-follower amplifier (column 8 line 47+).

Regarding claim 5, Yoneyama teaches that the row select signal generating circuitry generates the set of row select signals based on a row address signal that corresponds to a particular row and on a row aggregation control (composite) signal that corresponds to a number of rows in the selected corresponding set of plural particular rows (column 4 line 4+).

Regarding claim 6, Yoneyama teaches that row address signal generating circuitry that generates the row address signal (switching device controller).

Regarding claim 7, Yoneyama teaches that the row address signal generating circuitry generates the row address signal based, in part, on the row aggregation control signal (switching device generating composite signal).

Regarding claim 8, Yoneyama teaches that the set of row select signals is one set of row select signals in a sequence of sets of row select signals; the selected corresponding set of plural particular rows is one set of plural particular rows in a sequence of sets of plural particular rows; and the row select signal generating circuitry is configured to generate the sequence of sets of row select signals (column 4 line 4+).

Regarding claim 9, Yoneyama teaches that the row select signal generating circuitry generates the set of row select signals based on a row address signal that corresponds to a particular row; the row address signal is one row address signal in a

sequence of row address signals, the image sensor further comprises row address signal generating circuitry that generates the sequence of row address signals, each row address signal corresponding to a particular row; and the row select signal generating circuitry generates the sequence of sets of row select signals based on the sequence of row address signals and on a row aggregation control signal that corresponds to a number of rows in each selected corresponding set of plural particular rows (column 4 line 4+).

Regarding claim 10, Yoneyama teaches that the row address signal generating circuitry generates each next row address signal in the sequence based, in part, on the current row address signal (column 4 line 4+).

Regarding claim 11, Yoneyama teaches that the row address signal generating circuitry generates each next row address signal in the sequence based on the current row address signal and on the row aggregation control signal (column 4 line 4+).

Regarding claim 12, Yoneyama teaches that column select signal generating circuitry configured to generate a set of column select signals to substantially simultaneously select a corresponding set of plural particular columns such that the collective output signal for each column in the selected corresponding set of plural particular columns is substantially simultaneously provided to an output node of the image sensor (column 4 line 54+).

Regarding claim 13, Yoneyama teaches that the column select signal generating circuitry generates the set of column select signals based on a column address signal that corresponds to a particular column and on a column aggregation control signal that

corresponds to a number of columns in the set of plural particular columns (column 4 line 54+).

Regarding claim 14, Yoneyama teaches that column address signal generating circuitry that generates the column address signal (column 4 line 54+).

Regarding claim 15, Yoneyama teaches that the column address signal generating circuitry generates the column address signal based, in part, on the column aggregation control signal (column 4 line 54+).

Regarding claim 16, Yoneyama teaches that the set of column select signals is one set of column select signals in a sequence of sets of column select signals; the set of plural particular columns is one set of plural particular columns in a sequence of sets of plural particular columns; and the column select signal generating circuitry is configured to generate the sequence of sets of column select signals (column 4 line 54+).

Regarding claim 17, Yoneyama teaches that the column address signal is one column address signal in a sequence of column address signals; the image sensor further comprises column address signal generating circuitry that generates the sequence of column address signals, each column address signal corresponding to a particular column; and the column select signal generating circuitry generates the sequence of sets of column select signals based on the sequence of column address signals and on a column aggregation control signal that corresponds to a number of columns in each selected corresponding set of plural particular columns (column 4 line 54+).

Regarding claim 18, Yoneyama teaches that the column address signal generating circuitry generates each next column address signal in the sequence based, in part, on the current column address signal (column 4 line 54+).

Regarding claim 19, Yoneyama teaches that the column address signal generating circuitry generates each next column address signal in the sequence based on the current column address signal and on the column aggregation signal (column 4 line 54+).

Regarding claim 20, Yoneyama teaches an image sensor, comprising:

a plurality of active pixel sensors arranged into a plurality of rows and a plurality of columns, each active pixel sensor including a photo-sensor configured to generate a sensor signal nominally indicative of an intensity of light incident on the photo-sensor;

a follower-type amplifier configured to provide a buffered sensor signal based on the sensor signal; and

sensor output selection circuitry configured to selectively couple the buffered sensor signal to an output of the active pixel sensor when the row to which the active pixel sensor belongs is selected based on one of a set of row select signals corresponding to that row; for each column, a column line coupling together the outputs of the active pixel sensors that belong to that column and terminating in a column node for that column (column 8 line 57+);

row select signal generating circuitry configured to generate the set of row select signals to select a corresponding set of plural particular rows such that each active pixel sensor in the selected corresponding set of particular rows provides the buffered sensor

signal for that active pixel sensor to the column line for the column to which that active pixel sensor belongs; and column select signal generating circuitry configured to generate a set of column select signals to substantially simultaneously select a corresponding set of plural particular columns such that the column node for each column in the selected corresponding set of plural particular columns is substantially simultaneously coupled to an output node of the image sensor (column 3 line 60+).

Regarding claim 21, Yoneyama teaches that the column select signal generating circuitry generates the column select signals based on a column address signal that corresponds to a particular column and on a column aggregation control signal that corresponds to a number of columns in the selected corresponding set of plural particular columns (column 4 line 54+).

Regarding claim 22, Yoneyama teaches that column address signal generating circuitry that generates the column address signal (column 4 line 54+).

Regarding claim 23, Yoneyama teaches that the column address signal generating circuitry generates the column address signal based, in part, on the column aggregation control signal (column 4 line 54+).

Regarding claim 24, Yoneyama teaches that the set of column select signals is one set of column select signals in a sequence of sets of column select signals; the set of plural particular columns is one set of plural particular columns in a sequence of sets of plural particular columns; and the column select signal generating circuitry is configured to generate the sequence of sets of column select signals (column 4 line 54+).

Regarding claim 25, Yoneyama teaches that the column select signal generating circuitry generates the column select signals based on a column address signal that corresponds to a particular column; the column address signal is one column address signal in a sequence of column address signals; the image sensor further comprises column address signal generating circuitry that generates the sequence of column address signals, each column address signal corresponding to a particular column; and the column select signal generating circuitry generates the sequence of sets of column select signals based on the sequence of column address signals and on a column aggregation control signal that corresponds to a number of columns in each selected corresponding set of plural particular columns (column 4 line 54+).

Regarding claim 26, Yoneyama teaches that the column address signal generating circuitry generates each next column address signal in the sequence based, in part, on the current column address signal (column 4 line 54+).

Regarding claim 27, Yoneyama teaches that the column address signal generating circuitry generates the each next column address signal in the sequence based on the current column address signal and on the column aggregation signal (column 4 line 54+).

Regarding claim 30, Yoneyama teaches a camera, comprising:

an image sensor that includes a plurality of active pixel sensors arranged in a plurality of rows and a plurality of columns, each active pixel sensor including a photo-sensor configured to generate a sensor signal nominally indicative of an intensity of light incident on the photo-sensor;

a follower-type amplifier configured to provide a buffered sensor signal based on the sensor signal; and

sensor output selection circuitry configured to selectively couple the buffered sensor signal to an output of the active pixel sensor when the row to which the active pixel sensor belongs is selected based on a row select signal corresponding to that row; for each column, a column line coupling together the outputs of the active pixel sensors that belong to that column;

row select signal generating circuitry configured to generate the row select signals to substantially simultaneously select a set of plural particular rows such that each of the active pixel sensors in the selected set of plural particular rows substantially simultaneously provides the buffered sensor signal for that active pixel sensor to the column line for the column to which that active pixel sensor belongs, such that an output node of each column line indicates a collective output signal for the active pixel sensors in the selected set of plural particular rows, belonging to that column;

column select signal generating circuitry configured to generate column select signals to substantially simultaneously select a set of columns such that the collective output signal for each column in the selected set of columns is substantially simultaneously provided to an output node of the image sensor; a controller configured to control the row select signal generating circuitry and the column select signal generating circuitry; and

a memory configured to store signals provided at the output node of the image sensor (column 16 line 64+).

Regarding claim 31, Yoneyama teaches that a display device configured to display an image corresponding to the signals stored in the memory (solid state imaging device).

Regarding claim 32, Yoneyama teaches that the follower-type amplifier includes a field-effect transistor configured as a source-follower amplifier (column 8 line 47+).

Regarding claim 33, Yoneyama teaches that the sensor output selection circuitry includes a field-effect transistor, wherein the gate of the sensor output selection circuitry field-effect transistor is coupled to the one of the set of row select signals; and the source-follower amplifier field-effect transistor and the sensor output selection circuitry field-effect transistor each have the same conductivity type (column 8 line 47+).

Regarding claim 34, Yoneyama teaches that the follower-type amplifier includes a bipolar transistor configured as an emitter-follower amplifier (column 8 line 47+).

Regarding claim 35, Yoneyama teaches that the row select signal generating circuitry generates the set of row select signals based on a row address signal that corresponds to a particular row and on a row aggregation control signal that corresponds to a number of rows in the selected corresponding set of plural particular rows (column 4 line 4+).

Regarding claim 36, Yoneyama teaches that row address signal generating circuitry that generates the row address signal (column 4 line 4+).

Regarding claim 37, Yoneyama teaches that the row address signal generating circuitry generates the row address signal based, in part, on the row aggregation control signal (column 4 line 4+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoon K Song whose telephone number is 703-308-2736. The examiner can normally be reached on 8:30 AM - 5 PM, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 703-305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4858 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hoon K. Song
March 18, 2003

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